overview

CH233A-KG touch detection chip built-in voltage regulator circuit, provide stable voltage for touch sensing circuit use, stable touch detection effect can be widely used to meet the needs of different applications, this touch detection chip is designed to replace the traditional button and designed, the size of the touch detection PAD can be designed according to different sensitivity within a reasonable range, low power consumption and wide working voltage, is the characteristics of this touch chip in DC or AC applications.

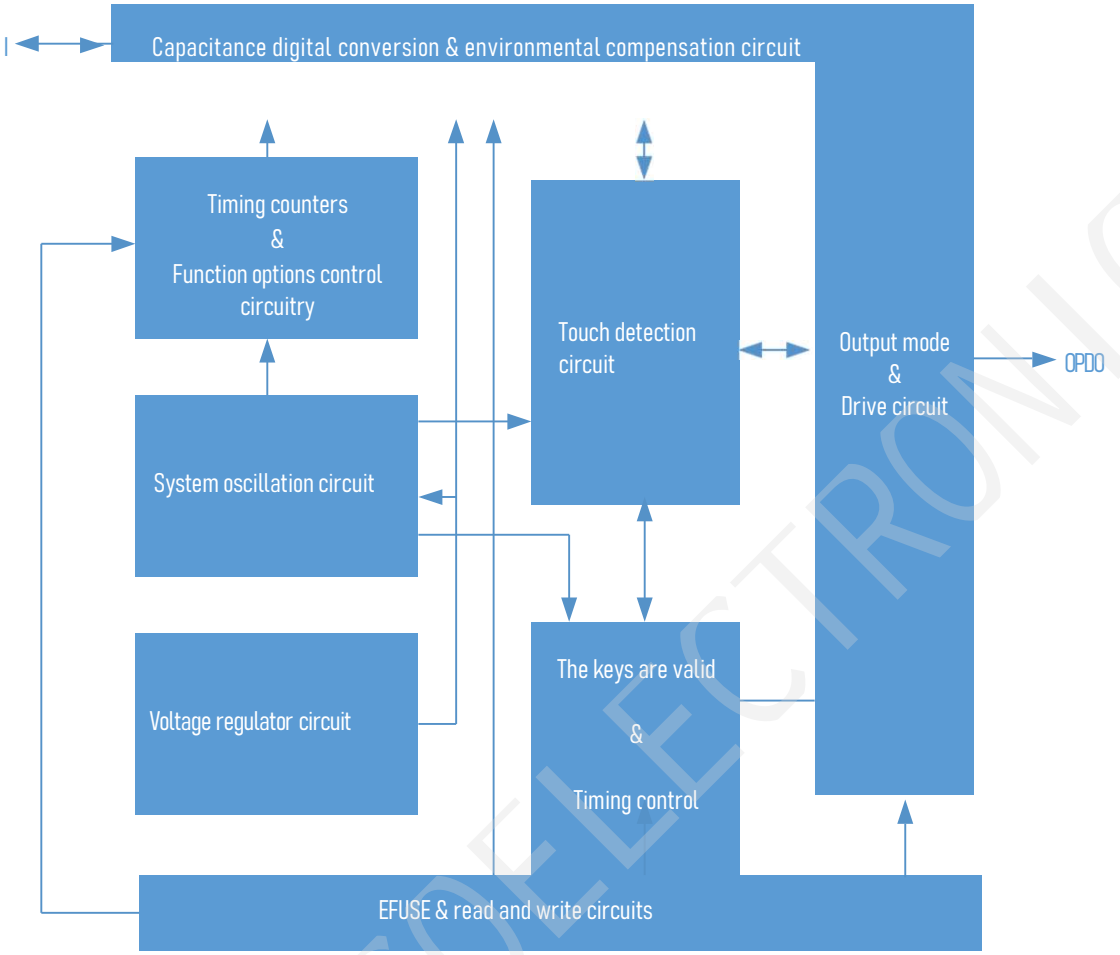
Features

- Operating voltage 2.3V ~ 5.5V
- The built-in voltage regulator circuit provides a stable voltage for the touch detection circuit, and the voltage regulator circuit can be shut down to save power consumption in environments with low reliability requirements
- Built-in Low Voltage Reset (LVR) function
- Operating current 2.4uA@VDD =3V, no load
- Sensitivity can be adjusted flexibly, no external capacitor is required, and the maximum parasitic capacitance value is 30pF
- Stable human touch detection replaces traditional key switches
- Provides the choice of normal key mode and delayed shutdown mode
- Synchronous mode and hold mode can be configured via EFUSE, eliminating the need for external selection resistors
- Provides a maximum output time of about 16 seconds @VDD = 3V
- The OPDO pin is a true open-drain output pin and is valid for low-level outputs
- There is a settling time of approximately 0.5 seconds after power-up, during which time the detection point is not touched, at which point all functions are disabled
- Automatic calibration function, environmental adaptive calibration function
- SOT23-6L package

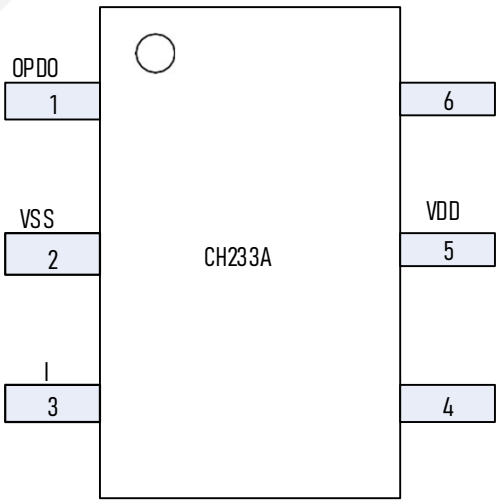
Scope of application

- A variety of consumer products
- Replaces the button keys

Block diagram



Pin arrangement diagram



PIN position definition

Foot position order	Pin name	I/O type	PIN position definition
1	OPDO	OD	True open drain pin, active low (ESD unilateral protection), output mode selection controlled by EFUSE
2	VSS	P	Negative power supply
3	I	I	Sensor input pin
4	/	/	Floating
5	VDD	P	Positive power supply
6	/	/	Floating

Pin type

I CMOS Single Pure Input /OD open leak input /P Power/Ground

Electrical characteristics

Maximum absolute rating

parameter	symbol	Conditions	value	unit
Operating temperature	T_{OP}	—	-40 ~ +85	℃
Storage temperature	T_{STG}	—	-50 ~ +125	℃
Power supply voltage	VDD	Ta=25 C	VSS-0.3 ~ VSS+5.5	V
Input voltage	V_{IN}	Ta=25 C	VSS-0.3 ~ VDD+0.3	V
Note: VSS stands for System Ground				

DC/AC characteristics (test conditions room temperature = 25℃)

parameter	symbol	Test conditions	minimum	Typical values	maximum	unit
Operating voltage	VDD		2.4	3	5.5	V
Internal regulator output	VREG		2.2	2.3	2.4	V
Operating current	I_{OPF}	VDD=3V low-power mode (no load.))		2.4	3	uA
Enter the foot	V_{IL}	Input low voltage	0		0.2	VDD

Enter the PIN	V_{IH}	Input high voltage	0.8		1.0	VDD
Output pin sink current Sink Current	I_{OL}	VDD=3V, V_{OL}=0.6V		8		mA
Output pin source current Source Current	I_{OH}	VDD=3V, V_{OH}=2.4V		-4		mA
Output response time	TR	VDD=3V、 Low-power mode		160		mS

Feature description

I. Sensitivity adjustment

The CH233A has built-in parasitic capacitance compensation circuitry that eliminates the need for external capacitance and adjusts the sensitivity by adjusting the value of the efuse register Proxth. The principle of ch233A guarantees that touch sensitivity remains consistent without the need for external capacitance and does not change with changes in the external environment. In addition to the CH233A's internal sensitivity adjustment circuitry, the CH233A provides a number of external methods for adjusting sensitivity。

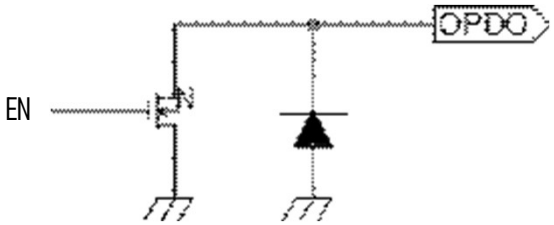
1. Resize the test plate size
2. Other things being equal, using a larger plate size increases sensitivity and vice versa decreases sensitivity, but electrode size must be used within the effective range.
3. 2. Adjust the media (panel) thickness
4. Other conditions remain the same, using a thinner medium increases sensitivity and vice versa decreases sensitivity; however, the thickness of the medium must be below the maximum limit.

II. Output mode (selected using the efuse register TOG)

TOG register: Direct output or toggle output can be selected in normal mode.

OPDO pin (open-drain output active low) option feature

TOG	Port OPDO option feature
0	Normal mode, direct mode, open-drain low active, power-up state is high impedance
1	Normal mode, toggle output, open-drain low active, high impedance power-up state



III. The maximum output time of the key

IV. In normal mode, if there is an object covering the detection board, it may cause enough to detect the amount of change, in order to avoid this situation, CH233A is equipped with a timer to monitor the detector, the timer is the maximum output duration of 16s, when detected beyond the timer time, the system will return to the initial state of power-up, and the output becomes invalid until the next detection.

V. Anti-interference capability selection

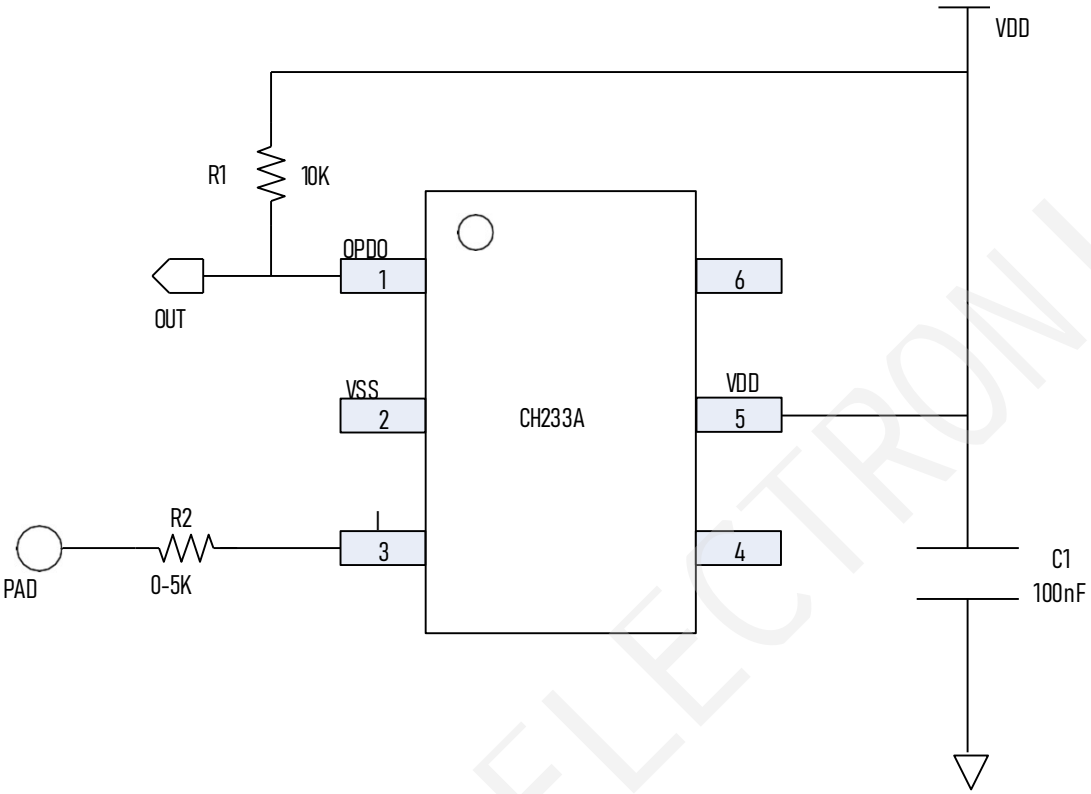
VI. CH233A has a strong anti-interference ability, can be used in places where interference is relatively large. The CH233A's immunity to interference is mainly adjusted by changing the EFUSE variable register, or the default configuration can be used. Customers can select the appropriate configuration for up-front commissioning via the recorder and commissioning software provided by us.

VII.

V. Efuse register description

VI. EFUSE data latches on and passes to registers, and the default value for EFUSE is 0 when EFUSE is not programmed。

Application circuits



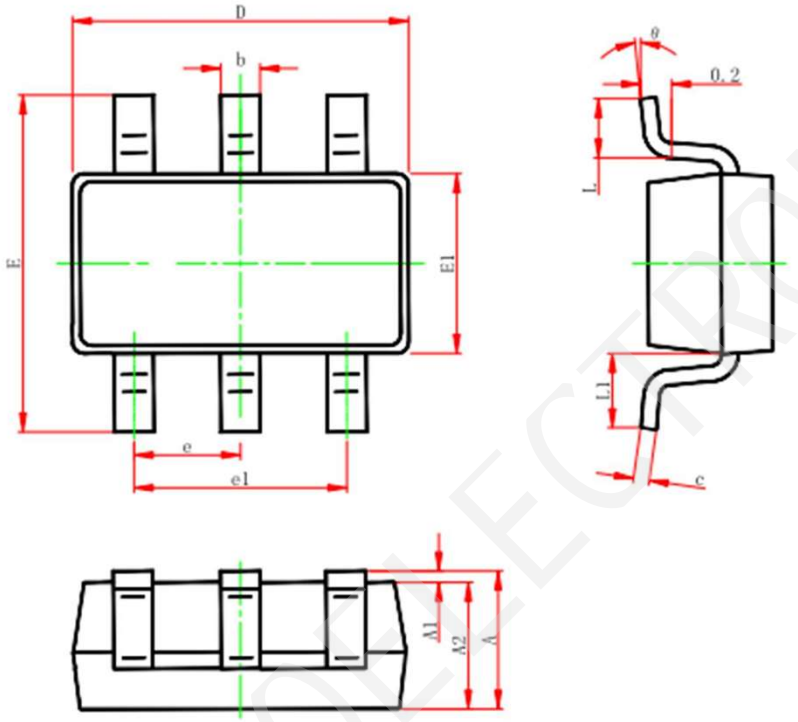
PS.

1. On a PCB, the shorter the line length from the touchpad to the IC pin, the better. And this wiring must not be parallel or crossed with other wires.
2. The power supply must be stable, and if the voltage supplied to the power supply drifts or drifts or shifts rapidly, it may cause abnormal sensitivity or mistesting.
3. The plates covered on the PCB must not contain ingredients of metal or conductive components, as well as surface coatings.
4. C1 capacitors must be used between VDD and VSS, and the shortest distance from the VDD and VSS pins of the device IC should be routed.

Package dimensions

Package type SOT23-6L

SOT-23-6L(12R) PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
L1	0.600REF.		0.024REF.	
θ	0°	8°	0°	8°