



CH177

Hingh Sensitivity CMOS utput Hall Effect Switch

Description

The CH177 is a Hall-effect latch designed in mixed-signal CMOS technology. The device integrates a voltage regulator, hall sensor with dynamic offset cancellation system, Schmitt trigger and an open-drain output driver or output with 8K Ohms upload resistor (Only available in Standard Magnetic Sensitivity), all in a single package.

Thanks to its wide operating voltage range and extended choice of temperature range, it is quite suitable for use in automotive, industrial and consumer application.

The device is delivered in a small outline transistor (SOT-23) for surface mount process, Quad Flat No-Lead Package (QFN2020-3) and TO-92 Plastic-encapsulate. Both 3-lead package are RoHS compliant.

Features

- Wide Operation Voltage Range Single supply voltage 3.5V to 30V
- Specified Operating Temperature Range: -50°C to 150 °C
- High Magnetic Sensitivity
- Chopper-Stabilized Amplifier Stage
- Open Drain Type Output
- 3-lead SOT-23 and TO-92S/QFN2020-3
- High ESD Capability 4KV HBM



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Pin Configuration

Table 1: Pin description for TO-92S

Pin No.	Pin Name	Function
1	VDD	Power supply
2	GND	Ground
3	OUT	Output

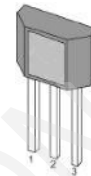


Table 2: Pin description for SOT-23

Pin No.	Pin Name	Function
1	VDD	Power supply
2	OUT	Output
3	GND	Ground

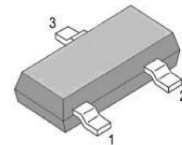


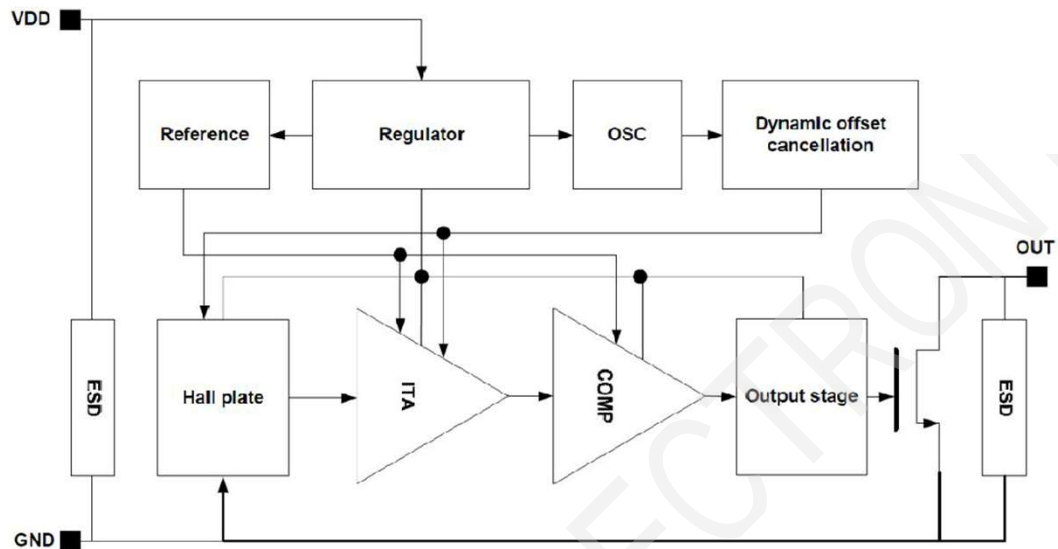
Table 3: Pin description for QFN2020-3

Pin No.	Pin Name	Function
1	VDD	Power supply
2	OUT	Output
3	GND	Ground





Block Diagram



Brief Theory of Operation

- Magnetic flux is transferred to a small voltage signal by the Hall device.
- Instrument amplifier amplifies the Hall voltage into a large swing signal.
- Dynamic offset cancellation system reduces the offset of Hall plate and amplifier.
- Hysteresis comparator converts the amplified signal into a switch signal as to the setting.
- Output stage latches the output of comparator, and drives an open-drain type output pin or output with 8K Ohms upload resistor (Only available in Standard Magnetic Sensitivity).



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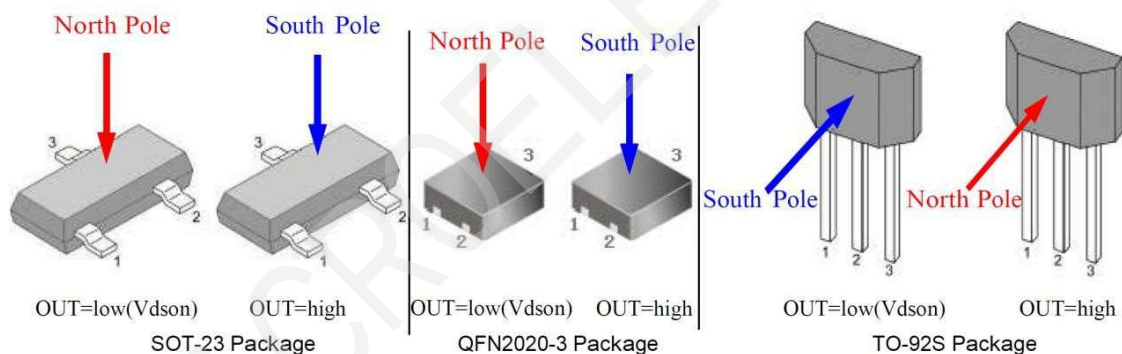
Definition of Magnetic Parameters

B_{OP}: Operating Point
Magnetic flux density applied on the branded side of the package which turns the output driver ON ($V_{out} = V_{DSon}$)

B_{RP}: Release Point
Magnetic flux density applied on the branded side of the package which turns the output driver OFF ($V_{out} = HIGH$)

B_{HYST}: Hysteresis Window $B_{OP} - B_{RP}$

Parameter	Test Condition (SOT-23)	OUT(SOT-23)	Test Condition (TO-92S/QFN2020-3)	OUT(TO-92S/QFN2020-3)
South Pole	$B < B_{RP}$	HIGH	$B > B_{OP}$	LOW
North Pole	$B > B_{OP}$	LOW	$B < B_{RP}$	HIGH



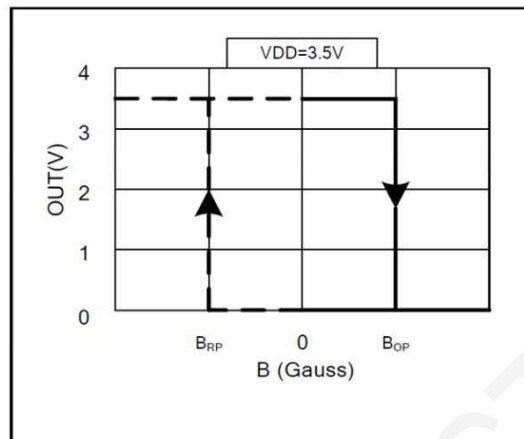
Latch characteristic

The CH177 device exhibits latch magnetic switching characteristics. Therefore, it requires both south and north poles to operate properly.

The device behaves as a latch with symmetric operating and release switching points ($B_{OP} = |B_{RP}|$). This means magnetic fields with equivalent strength and opposite direction drive the output high and low. Removing the magnetic field ($B \rightarrow 0$) keeps the output in its previous state. This latching property defines the device as a magnetic memory.



A magnetic hysteresis B_{HYS} keeps B_{OP} and B_{RP} separated by a minimal value. This hysteresis prevents output oscillation near the switching point.



Note:
 —→ South Pole
 - - -→ North Pole

Absolute Maximum Ratings

Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

Table 4 : Absolute maximum ratings (all voltages listed are referenced to GND)

Symbol	Parameters	Min	Max	Unit	Notes
T_s	Storage temperature	-50	150	°C	
T_j	Junction temperature	-50	150	°C	
VDD	Supply voltage		28	V	
I_{DD}	Supply current		50	mA	
V_{OUT}	Output voltage		28	V	
I_{OUT}	Continuous output current		50	mA	



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Electrical Characteristic

Table 5. Characteristics: at $T_a = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{DD} = 3.5$ to 30V , if not otherwise specified

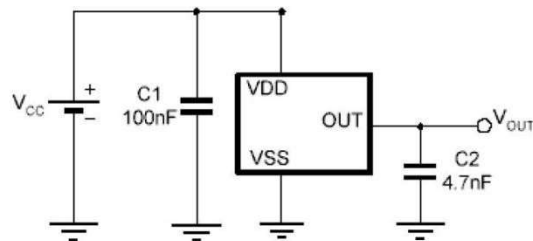
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	Note
Supply Voltage	VDD	Operating	3.5		30	V	
Supply Current	IDD	$B < B_{RP}$			5	mA	
Output Saturation Voltage	VDSN	$I_{OUT} = 20\text{mA}$, $B > B_{OP}$			0.5	V	
Output Leakage Current	IOFF	$R_L = 1\text{k}\Omega$, $C_L = 20\text{pF}$			10	μA	
Output Rise Time	T_R	$R_L = 1\text{k}\Omega$, $C_L = 20\text{pF}$			0.45	μS	
Output Fall Time	T_F				0.45	μS	
Max Switching Frequency	FSW	Single layer(1S) JEDEC board		10		KHz	
Package Thermal resistance	RTH			301		$^{\circ}\text{C/W}$	
Magnetic Operating Point	BOP		10		55	Gauss	standard Magnetic Sensitivity
Magnetic Release Point	BRP		-55		-10	Gauss	
Hysteresis Window	BHYST		60	80	100	Gauss	
Magnetic Operating Point	BOP		10		35	Gauss	High Magnetic Sensitivity
Magnetic Release Point	BRP		-35		-10	Gauss	
Hysteresis Window	BHYST		25	40	55	Gauss	
Electro-Static Discharge	ESD	HBM		4		KV	



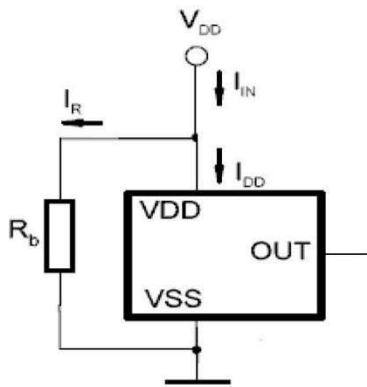
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Application Circuit



3-Wire Application Circuit



2-Wire Application Circuit

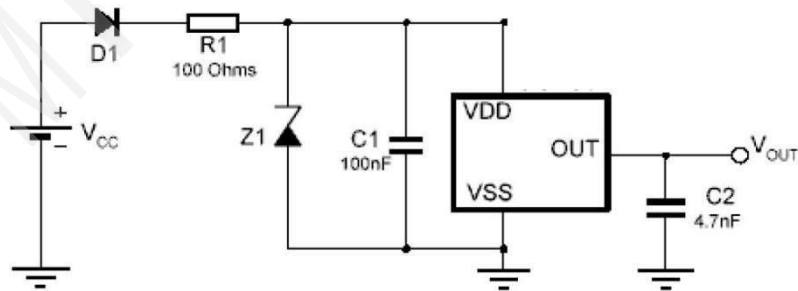
Note:

With this circuit, precise ON and OFF currents can be detected using only two connecting wires.

The resistors R_{pull} and R_b can be used to bias the input current. Refer to the part specifications for limiting values.

$$B_{RP}: I_{OFF} = I_R + I_{DDOFF} = V_{DD}/R_b + I_{DDOFF}$$

$$B_{OP}: I_{ON} = I_R + I_{DDON} = I_{OFF} + V_{DD}/10K$$



3-Wire Application Circuit For Harsh and Noisy Environment



Application Comments

For proper operation, a 100nF bypass capacitor should be placed as close as possible to the device between the VDD and ground pin.

For reverse voltage protection, it is recommended to connect a resistor or a diode in series with the VDD pin. When using a resistor, three points are important:

1. The resistor has to limit the reverse current to 50mA maximum ($V_{CC} / R_1 \leq 50\text{mA}$)
2. The resulting device supply voltage VDD has to be higher than VDD min ($V_{DD} = V_{CC} - R_1 \cdot I_{DD}$)
3. The resistor has to withstand the power dissipated in reverse voltage condition ($P_D = V_{CC}^2 / R_1$)

When using a diode, a reverse current cannot flow and the voltage drop is almost constant ($\approx 0.7\text{V}$). Therefore, a 100 Ohm/0.25W resistor for 5V application and a diode for higher supply voltage are recommended. Both solutions provide the required reverse voltage protection.

When a weak power supply is used or when the device is intended to be used in a noisy environment, it is recommended that a 3-wire application circuit for a harsh and noisy environment is used. The low-pass filter formed by R1 and C1 and the Zener diode Z1 bypass the disturbances or voltage spikes occurring on the device supply voltage VDD. The diode D1 provides additional reverse voltage protection.

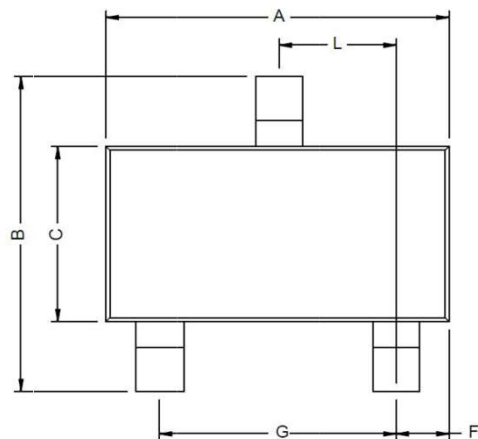


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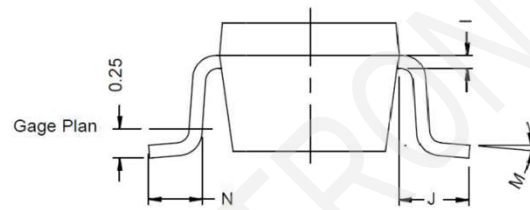
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Package information

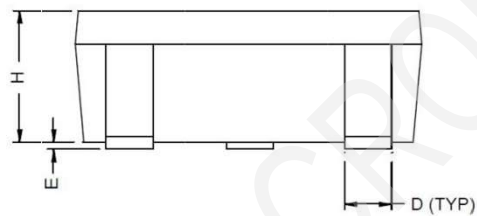
3-lead SOT-23 package diagram



Top View



End View



Side View

Dimensions

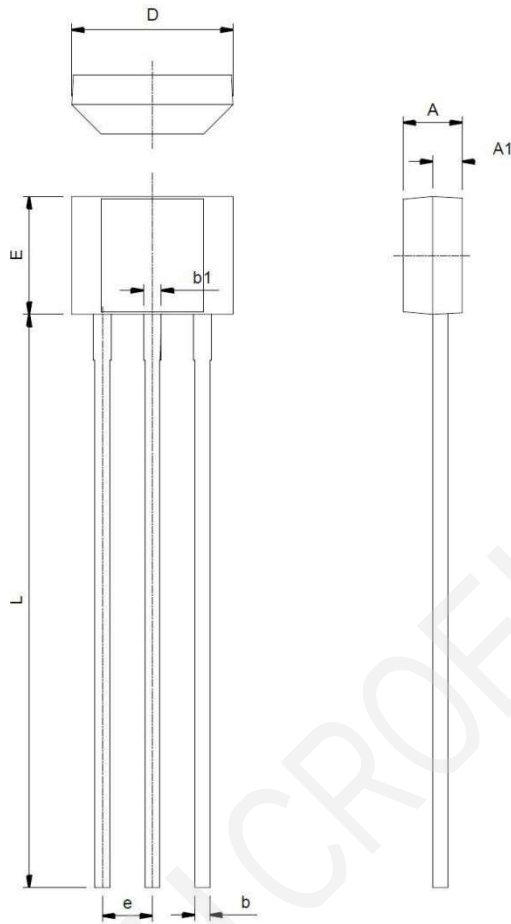
REF	Milimeter	
	Min	Max
A	2.70	3.10
B	2.40	2.80
C	1.40	1.60
D	0.35	0.50
E	0	0.10
F	0.45	0.55
G	2.10 REF	
H	1.00	1.30
I	0.10	0.20
J	0.40	-
L	0.95	1.15
M	0°	10°
N	0.30	0.60



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T0-92S package diagram



Dimensions

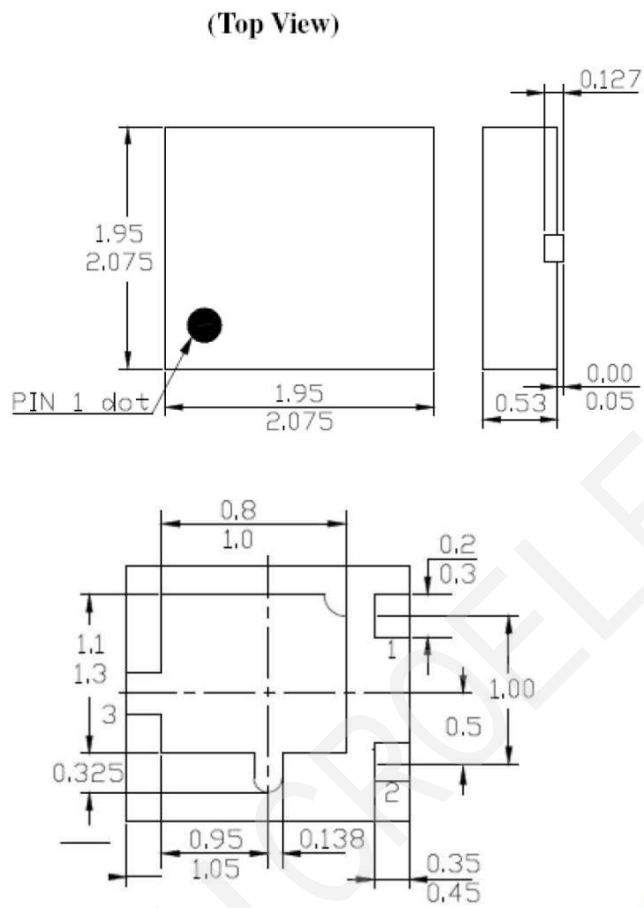
REF	Milimeter	
	Min	Max
A	1.245	1.753
A1	0.750 REF	
b	0.330	0.432
b1	0.406	0.508
D	3.962	4.216
E	2.870	3.164
L	13.60	15.60
e	1.270 REF	



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3-lead QFN 3 package diagram

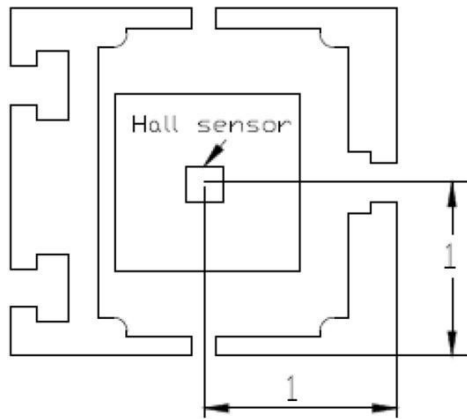




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(Bottom view)



Ordering Information

Part Number	Bop(GS)	Brp(GS)	Bhyst(GS)	Output	package
CH177AP	10~55	-10~-55	80	Opendrain	T0-92S
CH177AT	10~55	-10~-55	80	Opendrain	TSOT23-3
CH177AQ	10~55	-10~-55	80	Opendrain	QFN2020-3
CH177BP	10~55	-10~-55	80	Upload resistor	T0-92S
CH177BT	10~55	-10~-55	80	Upload resistor	TSOT23-3
CH177BQ	10~55	-10~-55	80	Upload resistor	QFN2020-3
CH177CP	10~35	-10~-35	40	Opendrain	T0-92S
CH177CT	10~35	-10~-35	40	Opendrain	TSOT23-3
CH177CQ	10~35	-10~-35	40	Opendrain	QFN2020-3